IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)
Shunpei YAMAZAKI et al.	) Attention: Applications Branch
Serial No. 09/837,558	)
Filed: April 19, 2001	)
For: SEMICONDUCTOR DEVICE AND	)
MANUFACTURING METHOD	)
THEREOF	)

RESPONSE TO NOTICE OF INCOMPLETE REPLAY

AND PRELIMINARY AMENDMENT

Honorable Commissioner for Patents

Washington, D.C. 20231

Sir:

In response to the Notice of Incomplete Reply – Filing Date Granted dated October 9, 2001 please preliminary amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 1-16 and add new claims 17-32 as follows:

--17. A semiconductor device including a CMOS circuit formed by n-channel TFT and p-channel TFT, characterized in that:

the CMOS circuit has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through an insulating layer in the n-channel TFT,

the active layer includes a low concentration impurity region that is in contact with the channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

18. A semiconductor device including a CMOS circuit formed by n-channel TFT and p-channel TFT, characterized in that:

the CMOS circuit has a structure that an active layer is sandwiched by a first

wiring line and a second wiring line through an insulating layer in the n-channel TFT and the p-channel TFT,

the active layer of the n-channel TFT includes a low concentration impurity region that is in contact with the channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

19. A semiconductor device according to claim 17, characterized in that the first wiring line of the n-channel TFT is electrically connected with the second wiring line.

20. A semiconductor device according to claim 17 or 18, characterized in that the first wiring line and/or the second wiring line is appropriately a conductive film mainly containing an element selected from the group consisting of tantalum (Ta) chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination.

21. A semiconductor device having a pixel TFT and a storage capacitor formed in the n-channel TFT, characterized in that:

the pixel TFT has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through an insulating layer,

the active layer includes a low concentration impurity region that is in contact with the channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

22. A semiconductor device according to claim 21, characterized in that the storage capacitor is formed between the first wiring line, the first insulating layer and the active layer.

23. A semiconductor device according to claim 21, characterized in that the first wiring line is kept at the floating electric potential.

24. A semiconductor device according to claim 21 or 22, characterized in that the first wiring line is kept at the lowest power supply electric potential.

25. A semiconductor device according to claim 21 or 22. characterized in that the first wiring line and/or the second wiring line is appropriately a conductive film mainly containing an element selected from the group consisting of tantalum (Ta). chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo). and silicon (Si), or an alloy film or silicide film containing the above elements in combination.

26. A semiconductor device having a pixel matrix circuit and a driver circuit that are formed on the same substrate. characterized in that:

a pixel TFT included in the pixel matrix circuit and an n-channel TFT included in the driver circuit have a structure that an active layer is sandwiched by a first wiring line and a second wiring line through an insulating layer; and

the first wiring line connected to the pixel TFT is kept at the lowest power supply electric potential, and the first wiring connected to the n-channel TFT included in the driver circuit is kept at the same level of electric potential as the second wiring line connected to the n-channel TFT included in the said driver circuit.

27. A semiconductor device according to claim 26, characterized in that the active layer includes a low concentration impurity region that is in contact with the channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

28. A semiconductor device according to claim 26 or 27. characterized in that the first wiring line and/or the second wiring line is appropriately a conductive film mainly containing an element selected from the group consisting of tantalum (Ta) chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo). and silicon (Si), or an alloy film or silicide film containing the above elements in combination.

29. A semiconductor device, characterized in that the semiconductor device according to any one of claims 17 is an active matrix liquid crystal display or an active matrix EL display.

30. A semiconductor device, characterized in that the semiconductor device according to any one of claims 17 is a video camera, a digital camera, a projector, a projection TV, a goggle type display, an automobile navigation system, a personal computer, or a portable information terminal.

31. Manufacturing method of a semiconductor device including a CMOS circuit formed by n-channel TFT and p-channel TFT comprising:

a process of forming a first wiring line on a substrate,

a process of forming a first insulating layer on the first wiring line,

a process of forming an active layer of the n-channel TFT and an active layer of the p-channel TFT on the first insulating layer,

a process of forming a second insulating layer by overlapping the active layer of n-channel TFT and the active layer of p-channel layer, and

a process of forming a second wiring line on the second insulating layer,

a process of forming a LDD region on the active layer of the n-channel TFT; and

the LDD region is provided overlap the first wiring line and not to overlap the second wiring line.

32. Manufacturing method of a semiconductor device according to claim 31, characterized in that the first wiring line and! or the second wiring line is formed by a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination. --

REMARKS

In response to the Notice to Incomplete Reply – Filing Date Granted, a copy submitted herewith, this application has been amended to correct minor informalities to comply with 37 CFR 1.75(h). Specifically, claims 1-16 have been canceled and new claims 17-32 have been added so that the claims commence on a separate sheet. Examination on the merits is requested.

Respectfully submitted,

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